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THD Analysis of Cascaded H-Bridge With Level Shifted Multicarrier Modulation

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Abstract: *A discussion on main topologies of multilevel inverter namely H Bridge, NCP (neutral point clamped) and flying capacitor is carried out utilizing carrier based PWM methods. The H-bridge inverter is mainly focused as it eliminates the excessively large number of (i) transformers required by conventional multilevel inverters (ii) one of the popular topology used in high power medium voltage drive .So evaluation is done on basis of total harmonic component (THD) in 3, 5 and7 level cascaded H-bridge topology using different PWM namely PD, POD, APOD respectively. Purpose of different modulation techniques is to ensure smoother operation of drives as it lowers the THD. The detailed study is carried out using MATLAB software.*

Keywords: Multilevel inverter, PWM, THD, NCP, cascaded H-bridge.

1. INTRODUCTION

Over past decade, multilevel inverter(MLI) come as revolution in field of inverter technology[1,2],as their application to medium and high level voltage is remarkable(2-13kV) which includes ac drives[3],power distribution[4],PV application[5],electric vehicle[6]etc. Main advantages of MLI: (a) reduction of input voltage stress on component thereby reducing voltage rating of device (b) decrease in conduction time, (c) lower device switching frequency for same number of output voltage level ultimately reducing the THD. Apart of these advantages its disadvantage are (a) complex circuit, (b) problem of voltage balance, (c) high cost etc. This paper helps in understanding the output voltage characteristics of 3, 5 and 7 level cascaded H Bridge subjected to different carrier PWM techniques.

2. MAJOR TOPOLOGIES OF MLI

A. Neutral Point Clamped(NPC)

It is proposed by A.NABAE, I.TAKAHASHI and H.AKAGI [7,8].The incoming dc voltage is common for all phases and is splitted into(m-1) equal level there by providing neutral points. The given 3 level NPC configuration does not include capacitor because it has a problem of capacitor voltage balancing which require a control strategy .In practical scenarios for higher voltage rating the diode should bear that voltage so large a number of diode is required therefore NPC is used to three level usually for practical purpose.

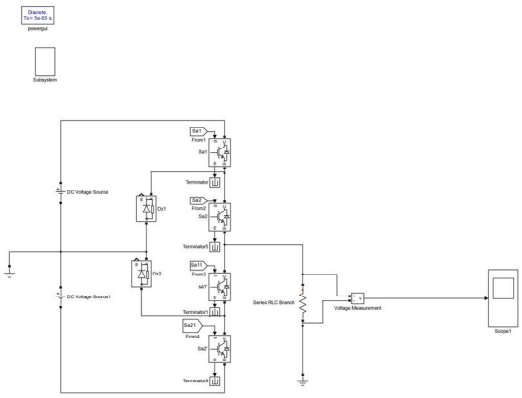


Figure 1. Phase A of 3-Level NPC.

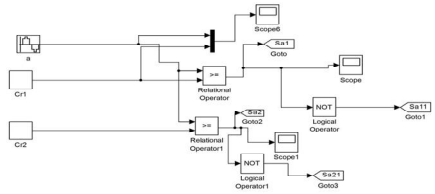


Figure 2.Switching sub system of 3-Level NPC.

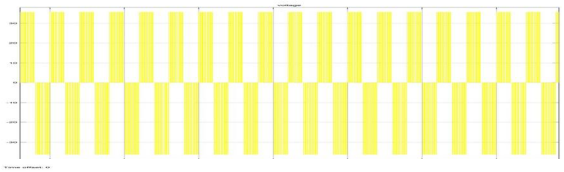


Figure 3.Voltage wave form of 3-Level NPC.

B. Flying Capacitor

Introduced by MEYNAR AND FOCH [9], Its working is identical to NPC only contrast is it uses capacitor in place of clamping diodes. The only ease of this topology is its less complexity and can be easily used for higher voltage rating, although bulky nature of capacitor, problem of voltage balance and thus complex control strategy make its use less common in industrial applications.

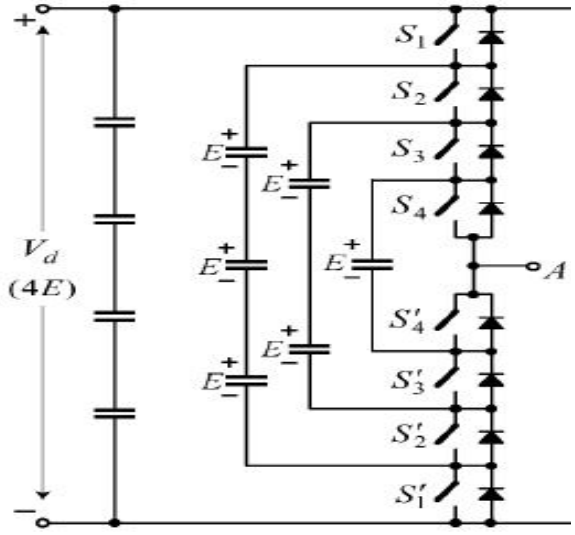


Figure 4. 5-level FLYING CAPACITOR inverter for phase-A.

C. Cascaded H Bridge

It is composed of two inverter legs with two IGBT devices in each leg[10]. Each level can be obtained by connecting dc source to ac output by proper combination of switches (i) number of output level m=2s+1 where s=number of dc source.

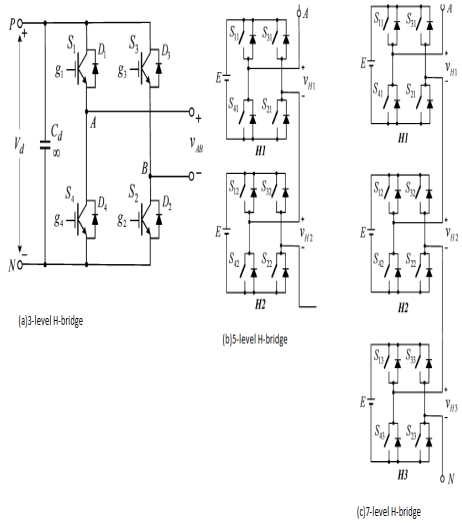


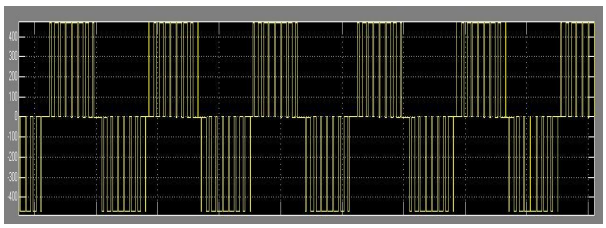
Figure5. 3, 5, 7-Level H-bridge inverter

The inverter phase voltage is given as

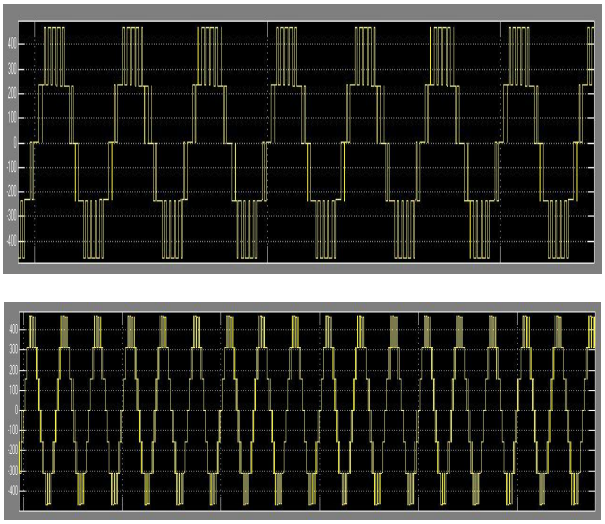
$$vAN = vH1 + vH2 + vH3$$

H-bridge requires a number of isoated dc suppies which make it suitable converter of distributed generation supplies i.e power from batteries ,fuel cell ,photovoltaic cell can be united under one roof.

The upper and lower switches in each leg operates in complementary mode so for three level we require two gate signals for S1 and S3 which are generated by comparing the sinusoidal wave by the two triangular carrier wave as shown in the sub sustem. Since the wave form of voltage between terminal A and B switches between the positive and negative dc voltage Vd, this scheme is known as bipolar modulation.If the incoming dc voltages are all same then it is known as symmetrical H-bridge configuration otherwise it is is known as asymmetrical H-bridge configuration.



a



b

C

Figure6 output waveform of (a)3-level,(b)5-level,(c)7-level

When switches S_{11}, S_{21}, S_{12}, and S_{22} conduct, the output voltage of the H- bridge cells *H1* and *H2* is $v_{H1} = v_{H2} = E$, and the resultant **inverter phase voltage** is $v_{AN} = v_{H1} + v_{H2} = 2E$, which is the voltage at the inverter terminal *A* with respect to the inverter neutral *N*. Similarly, with S_{31}, S_{41}, S_{32}, and S_{42} switched on, $v_{AN} = -2E$.

The number of voltage levels in a CHB inverter can be found from

$$m = (2H + 1)$$

Where *H* is the number of H-bridge cells per phase leg.

The total number of **active switches** (IGBTs) used in the CHB inverters can be calculated by

$$N_{SW} = 6(m - 1)$$

Where *m* is the number of H-bridge cells.

3. VARIOUS CARRIER BASED PWM TECHNIQUES

A. Phase Shift Modulation

In general, a MLI with m-level need (m-1) triangular carriers. All the triangular carriers have the same frequency and same peak to peak amplitude in phase shifted multicarrier modulation but the carriers have a phase shift as follows

$$Øcr = 360°/(m - 1)$$

The modulating signal is usually 3-phase sinusoidal wave with adjustable amplitude and frequency. By comparing carrier waves with modulating wave gate signals are generated

-for 3 level

$$Øcr = 360°/(m-1) = 360°/(3-1) = 360°/2 = 180^0$$

-for 5 level

$$Øcr = 360°/(m-1) = 360°/(5-1) = 360°/4 = 90^0$$

B. Level Shifted

It requires (m-1) carriers for m level inverter which are vertically disposed. Amplitude modulation index is defined as

$$ma = Vm / Vcr(m - 1) \quad \text{for } 0 <= ma <= 1$$

Where

Vm is the peak amplitude of the modulating wave

Vcr is the peak amplitude of each carrier wave.

Three scheme for level shifted are

(A) Phase disposition (PD), this scheme employs all carriers in phase.

(B) Phase opposite disposition (POD), this scheme employs carrier above and below zero point with phase shift of 180.

(C) Alternate phase opposite disposition (APOD), this scheme employs carrier phase shifted by 180 from its adjacent carrier.

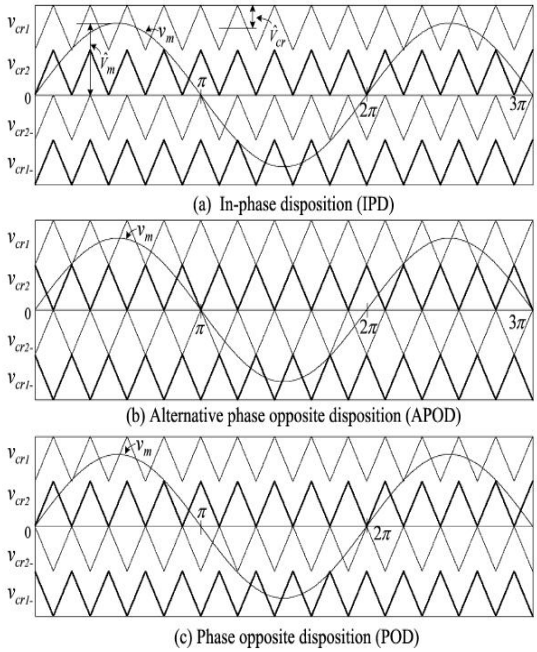


Figure7 Level shifted for 5 level inverter

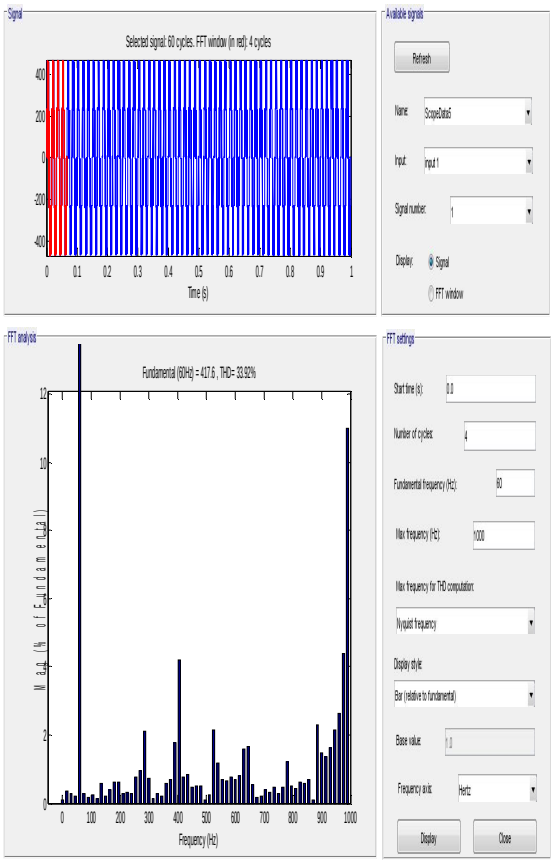


Figure8.THD result of 3-Level H-bridge.

4. Results

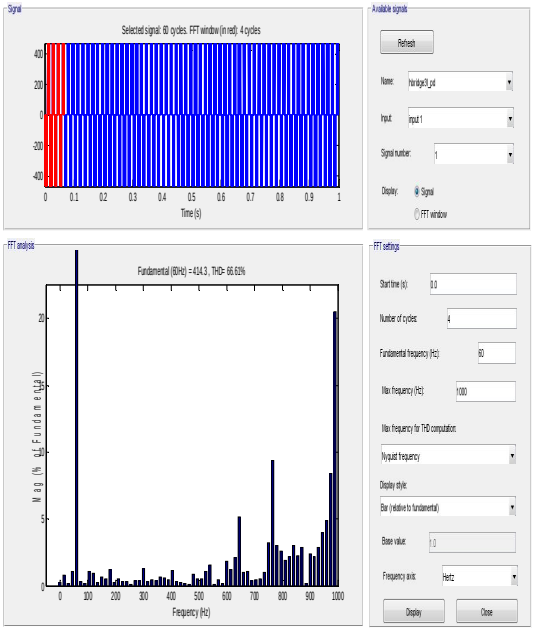


Figure9.THD result of 5-LevelH-bridge

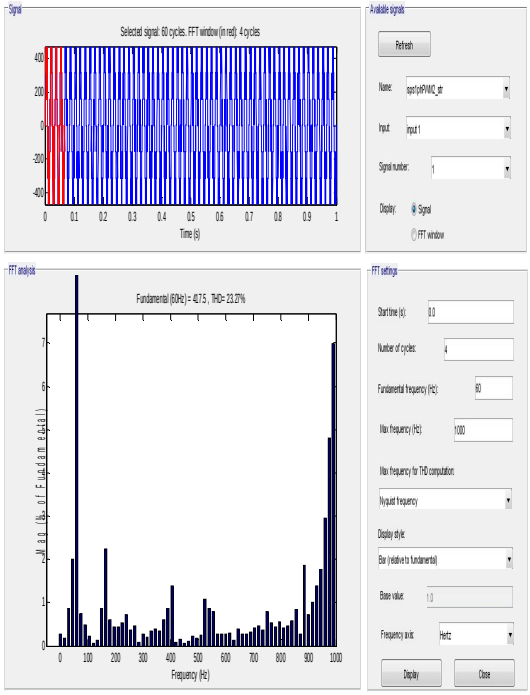


Figure10.THD result of 7-Level H-bridge

NU. OF LEVEL	PD (in %)	POD (in%)	APOD(in%)
3	66.71	65.97	N/A
5	33.92	33.71	33.56
7	23.27	22.87	23.22

Table no 1. THD comparison of 3, 5, 7 Level H bridge using Various Level shifted PWM techniques.

4. CONCLUSION

This paper discuss about performance characteristics of various cascaded H Bridge utilizing various PWM input (PD, POD, APOD). Comparison of THD level components is also tabulated which shows by increasing number of level THD reduced to a great extent and it also show that it is minimum for 7 Level using POD PWM scheme.

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